

WHAT IS CLAIM IS:

1 1. An a-WO₃ gate ISFET device, comprising:
2 a semiconductor substrate;
3 a gate oxide layer on the semiconductor substrate;
4 an a-WO₃ layer overlying the gate oxide layer to form
5 an a-WO₃ gate;
6 a source/drain in the semiconductor substrate beside
7 the a-WO₃ gate;
8 a metal wire on the source/drain; and
9 a sealing layer overlying the metal wire, and
10 exposing the a-WO₃ layer.

1 2. The device as claimed in claim 1, wherein the
2 length of the channel, the width of the channel and ratio of
3 width/length of the channel of the ISFET is about 50μm, 1000μm,
4 and 20 respectively.

1 3. The device as claimed in claim 1, wherein the
2 semiconductor substrate is P-type.

1 4. The device as claimed in claim 1, wherein the
2 resistivity of the semiconductor substrate ranges from 8 to
3 12 Ω·cm.

1 5. The device as claimed in claim 1, wherein the
2 lattice parameter of the semiconductor is (1,0,0).

1 6. The device as claimed in claim 1, wherein the
2 thickness of the gate oxide is about 1000Å.

1 7. The device as claimed in claim 1, wherein the
2 thickness of the tungsten oxide layer is at least 1000Å.

1 8. The device as claimed in claim 1, wherein the metal
2 wire consists of Al.

1 9. The device as claimed in claim 1, wherein the
2 sealing layer consists of epoxide resin.

1 10. The device as claimed in claim 1, wherein the
2 source/drain is N-type.

1 11. The device as claimed in claim 10, wherein the
2 N-type impurities within the source/drain consist of
3 phosphorous.

1 12. A method for fabricating an a-WO₃ gate ISFET
2 device, comprising the following steps:
3 providing a semiconductor substrate;
4 forming an imaginary gate on the semiconductor
5 substrate to define the gate area of the ISFET;
6 forming a source/drain in the semiconductor
7 substrate beside the imaginary gate;
8 removing the imaginary gate; and
9 forming an a-WO₃ gate in the gate area to form a ISFET.

1 13. The method as claimed in claim 12, wherein the
2 semiconductor substrate is P-type.

1 14. The method as claimed in claim 12, wherein the

2 resistivity of the semiconductor substrate ranges from 8 to
3 12 $\Omega \cdot \text{cm}$.

1 15. The method as claimed in claim 12, wherein the
2 lattice parameter of the semiconductor is (1,0,0).

1 16. The method as claimed in claim 12, wherein the
2 imaginary gate consists of silicon dioxide.

1 17. The method as claimed in claim 12, wherein the
2 thickness of the imaginary gate is about 5000Å.

1 18. The method as claimed in claim 12, wherein the
2 imaginary gate is removed by means of wet-etching.

1 19. The method as claimed in claim 12, wherein the
2 step of forming an imaginary gate in the semiconductor gate
3 to define a gate area of the ISFET comprises:

4 cleaning the semiconductor substrate;

5 forming a pad oxide layer on the semiconductor
6 substrate; and

7 removing a portion of the pad oxide layer to form an
8 imaginary gate to define the area of the gate.

1 20. The method as claimed in claim 19, wherein the
2 pad oxide layer is formed by means of wet oxidation.

1 21. The method as claimed in claim 19, wherein the
2 step of removing a portion of the pad oxide layer is completed
3 by means of wet etching.

1 22. The method as claimed in claim 12, wherein the
2 step of forming a source/drain beside the imaginary gate
3 comprises:

4 doping the semiconductor substrate by using the
5 imaginary gate as a mask to form a source/drain.

1 23. The method as claimed in claim 22, wherein the
2 dose of the dopants is about 10^{15} atoms/cm².

1 24. The method as claimed in claim 12, wherein the
2 step of forming an a-WO₃ gate in the gate area comprises:
3 forming a gate oxide layer on the gate area; and
4 forming an a-WO₃ layer on the gate oxide to form a a-WO₃
5 gate.

1 25. The method as claimed in claim 24, wherein the
2 thickness of the gate oxide layer is about 1000Å.

1 26. The method as claimed in claim 24, wherein the
2 gate oxide consists of silicon dioxide.

1 27. The method as claimed in claim 24, wherein the
2 a-WO₃ gate is formed by RF-sputtering.

1 28. A method for fabricating an a-WO₃ gated ISFET,
2 comprising following steps:
3 providing a P-type semiconductor substrate;
4 forming a pad oxide layer on the semiconductor layer;
5 removing a portion of the pad oxide layer to form an
6 imaginary gate to define a gate area;

7 doping the semiconductor substrate by using the
8 imaginary gate as a mask to form a source/drain beside the
9 imaginary gate;
10 removing the imaginary gate;
11 forming a gate oxide layer on the semiconductor
12 substrate; and
13 forming an a-WO₃ layer on the gate oxide layer to form
14 an a-WO₃ gate.

1 29. The method as claimed in claim 28, wherein the
2 resistivity of the semiconductor substrate ranges from 8 to
3 12 $\Omega \cdot \text{cm}$.

1 30. The method as claimed in claim 28, wherein the
2 lattice parameter of the semiconductor is (1,0,0).

1 31. The method as claimed in claim 28, wherein the
2 thickness of the imaginary gate is about 5000Å.

1 32. The method as claimed in claim 12, wherein the
2 pad oxide layer is formed by means of wet oxidation.

1 33. The method as claimed in claim 28, wherein the
2 step of partially removing the pad oxide layer is performed
3 by wet etching.

1 34. The method as claimed in claim 28, wherein the
2 dopants used for doping consist of phosphorous.

1 35. The method as claimed in claim 28, wherein the

2 dose of the dopants is 10^{15} atoms/cm².

1 36. The method as claimed in claim 28, wherein the
2 imaginary gate is removed by wet etching.

1 37. The method as claimed in claim 28, wherein the
2 gate oxide layer consists of silicon dioxide.

1 38. The method as claimed in claim 28, wherein the
2 thickness of the gate oxide layer is about 1000Å.

1 39. The method as claimed in claim 28, wherein the
2 a-WO₃ layer is formed by RF-sputtering.